# Aflevering 3

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Indholdsfortegnelse

[Aflevering 3 1](#_Toc185010368)

[Question 1. Rin & Rout for the circuit 2](#_Toc185010369)

[Question 2. Rin & Rout for the circuit 7](#_Toc185010370)

[Question 3 11](#_Toc185010371)

[a. Find the DC value of Vin, that will give a dc current in M1 of . 11](#_Toc185010372)

[b. Calculate the small signal voltage gain and output resistance. 12](#_Toc185010373)

[Question 5. Biasing, gain and impedance 13](#_Toc185010374)

[c. Find the minimum required Vbias2. 13](#_Toc185010375)

[d. What is the small-signal voltage gain of the circuit? 14](#_Toc185010376)

[e. Calculate input and output impedance. 16](#_Toc185010377)

[Question 6. Calculate the gain of the following circuit. Provide the expression of the gain in terms of circuit parameters. 17](#_Toc185010378)

[f. At very low frequencies 17](#_Toc185010379)

[g. At very high frequencies 18](#_Toc185010380)

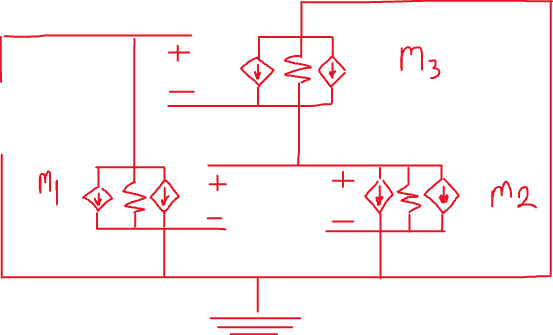
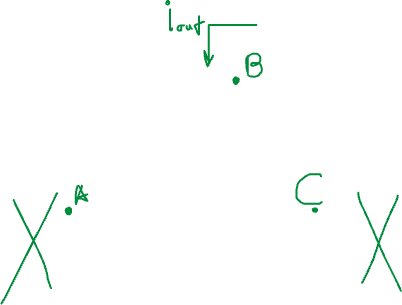
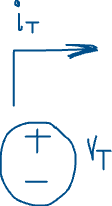
[h. Calculate the poles and the amplifier transfer function. 19](#_Toc185010381)

[c. Calculate the poles and the amplifier transfer function. 20](#_Toc185010382)

## Et billede, der indeholder diagram, tekst, skærmbillede, linje/række Automatisk genereret beskrivelseQuestion 1. Rin & Rout for the circuit

Determine the expression for input impedance Rin and output impedance Rout for the following circuit.

For this I will implement a test voltage at the input, and then at the output and in both cases look at what the resistance, the current sees, is.   
Finding the input impedance:



# Current over rO3 is opposite the others

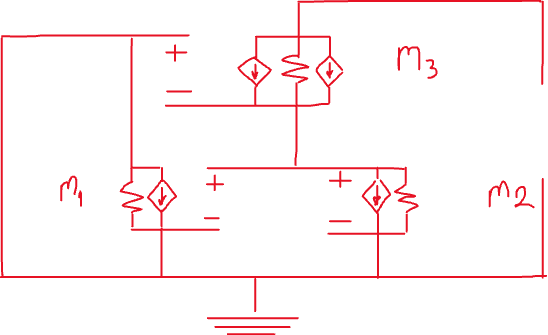
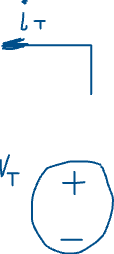
Substituting the content of the equations:

And now it’s clear, that the current through the internal resistance might lead to an opposite current contribution.   
   
   
   
   
   
   
   
   
  
   
   
  
Simplifying:

Suggesting that for all transistors.   
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Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelseOutput impedance:



Substituting 3 equation for VC.  
   
   
Substituting into equation 2.   
   
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As the first test voltage applied a test voltage to the M1, that was waiting for the output circuit to respond, for it to allow for current flow, 3 equations was needed. Now for this test voltage I only care about the right side, as the left side doesn’t gate my right side. That’s why I didn’t need my 1st equation.

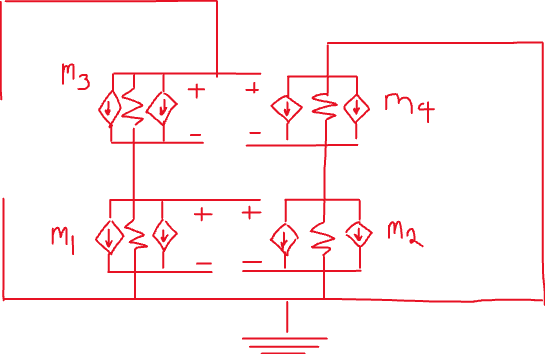
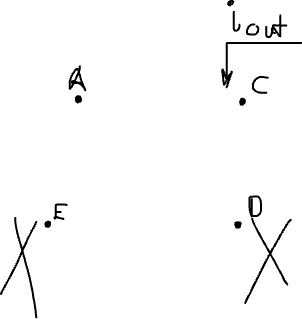
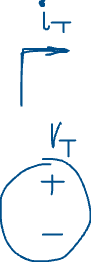
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## Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan Automatisk genereret beskrivelseQuestion 2. Rin & Rout for the circuit

Determine the expression for input impedance Rin and output impedance Rout for the following circuit.

As where the first problem had an feedback from the output side to the input side, the feedback is now only at the input side.   
***Input impedance***



Et billede, der indeholder tekst, skærmbillede, Font/skrifttype, linje/række

Automatisk genereret beskrivelseSolving for VD, then VE for a start.   
For eq. 4

Substituting into eq. 3  
   
   
   
   
   
  
Substituting into equation 2. Seems as these expressions are getting a little to large for comfort. Using python to solve them for me.  
Checking the results for solving eq. 4 for VD, eq.3 for VE

It seems as I’ve came to the same conclusions.

Now substituting into equation 2 to solve for iOut.   
Et billede, der indeholder tekst, Font/skrifttype, skærmbillede, linje/række

Automatisk genereret beskrivelse  
It’s a nice expression of VT factorized onto it all.

Now substituting equation VE into equation 1, then substituting iOut to get the equation for the impedance.   
I get a large equation containing:

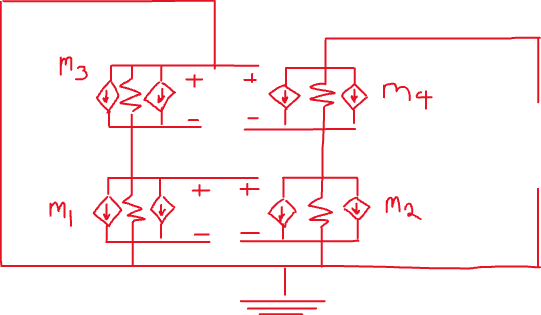
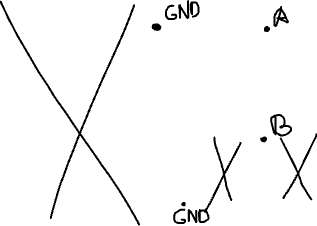
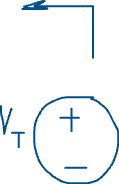
Et billede, der indeholder tekst, Font/skrifttype, skærmbillede, nummer/tal

Automatisk genereret beskrivelseI’m not sure how valid my final result is. I had a whole screen filled with the equation for Rin, but by simplifying it, I could boil it down to:

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This implies, the input only feels resistance from the gm3 and ro3, which seems odd.

***Output impedance.***As input side is grounded no voltage will be over the left hand side.  
If the source of m2 had been different than GND, then a voltage on the input side could have been on there.



So the only part from the 2nd transistor is the internal resistance.

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So the input and output resistances for the circuit, respectively:  
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## Question 3Et billede, der indeholder diagram, Font/skrifttype, Teknisk tegning, Plan Automatisk genereret beskrivelse

Assume that W/L in the following circuit are:



And use

### Find the DC value of Vin, that will give a dc current in M1 of .

Assuming M1 to be in saturation:

Finding Vout from:   
Setting to our default for pmos

Et billede, der indeholder tekst, skærmbillede, Font/skrifttype, sort

Automatisk genereret beskrivelseWhere any of these describes the relationship between VDD and gate of m4.

One reasonable one, as having more voltage at the gate than at the source doesn’t make sense.

Now I know the gate voltage of m3 and I know the source voltage as vout. I should then be able to solve for Vout.

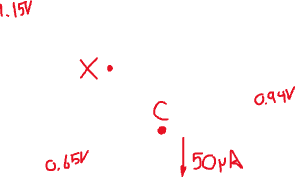
*Ligningen løses for V\_out vha. WordMat.*

That doesn’t make sense, something must have gone wrong.

### Calculate the small signal voltage gain and output resistance.

## Question 5Et billede, der indeholder diagram, Plan, linje/række, Teknisk tegning Automatisk genereret beskrivelse. Biasing, gain and impedance

In the following circuit assume that:



Furthermore, assume that:

### Find the minimum required Vbias2.

For a bias always to run, the vbias must secure all current in the circuit, in the case, that the input transistor is off.   
Assuming, that Vbias2 is setup for saturation.

To find VGS, we need the source node aswell. I’ll call it C.   
Assuming, that Vbias1 is setup for saturation.

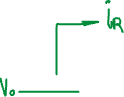
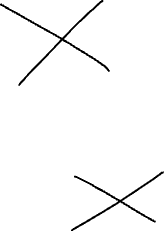
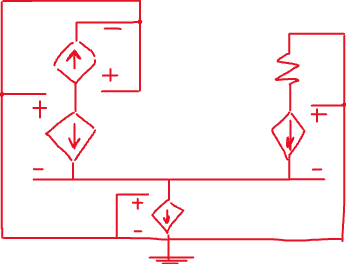
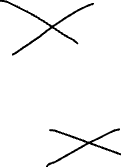
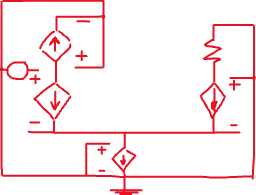
These assumption are reasonable, cause they’ll ensure me, that even if C were to become larger for some reason, say a change in VDD, the bias current would still be 50 micro amps, as no channel length modulation happens.

So the minimum drains source voltage is found at  
   
   
  
Giving it around 10% in wiggle room:

Now solving for the first equation.   
   
   
   
   
   
About 5% in wiggle room.   
   
Making the required bias voltage be:   
   
   
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### What is the small-signal voltage gain of the circuit?

So the only path for current to run is throught the   
 transistor.   
   
   
 What about the  
 transconductance?   
‘’’



The path now goes from the input transistor  
through m2 and into ground.   
   
   
   
   
   
   
   
  
  
   
For gm2 never experience change in current.  
   
   
Now for gm1:



If keep in saturation, as I assumes.

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### Calculate input and output impedance.

I’ve already calculated the output impedance to be   
   
Now for the input impedance, as it’s the “input” with a cross beneath the input, I describe the input current as the one entering the gate.   
As for the mosfet, it’s ideal input impedance is ideally close to infinity, this is what I will consider my answer.   
   
  
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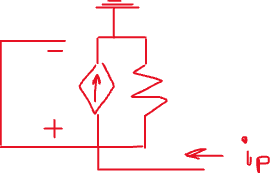
## Question 6. Calculate the gain of the following circuit. Provide the expression of the gain in terms of circuit parameters.

In this problem, neglect all other capacitances that aren’t shown in the circuit and assume for all three transistors, while

This means

### Et billede, der indeholder tekst, skærmbillede, diagram, linje/række Automatisk genereret beskrivelse At very low frequencies

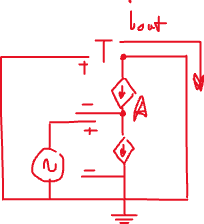
This acts as a diode connected pmos, and a cascode nmos network.







For the transconductance, no currents will flow through the pmos network.



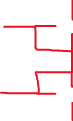
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Et billede, der indeholder tekst, skærmbillede, diagram, linje/række

Automatisk genereret beskrivelse

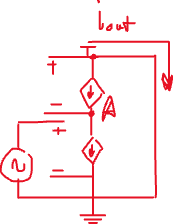
### At very high frequencies

For small signal bias is grounded, then   
As the input transistor is grounded then:   
   
And as and , no currents will run through the input transistor.   
And thus no currents will run through the nmos network.

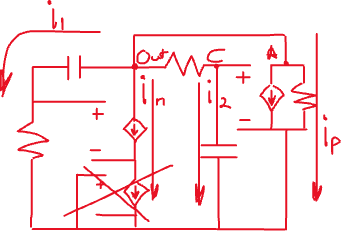


As pmos has ground at gate  
   
And the only resistance seen is

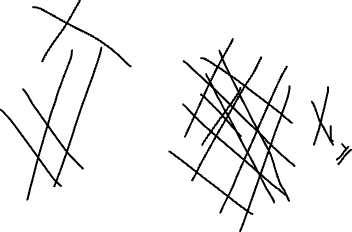
For the transconductance:   
   
   
   
   
   
   
   
   
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### Et billede, der indeholder tekst, skærmbillede, diagram, linje/række Automatisk genereret beskrivelseCalculate the poles and the amplifier transfer function.



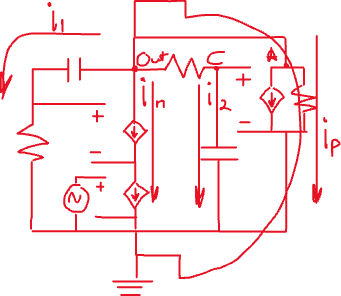
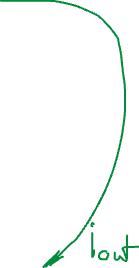
Now for the transconductance:   
No currents will flow otherwhere else  
than at the nmos network to the  
outputted ground.



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The solutions are insanely large, so some further simplification must be done, I thinkEt billede, der indeholder tekst, skærmbillede, diagram, kredsløb

Automatisk genereret beskrivelseEt billede, der indeholder tekst, skærmbillede, Font/skrifttype, sort

Automatisk genereret beskrivelse



*New approach:*

### c. Calculate the poles and the amplifier transfer function.

Still using:

Instead of observing the circuit as a hole, let me instead break it down into the paths and how they will get effected.   
And that is for both path 1 and 2.

For the pmos path

*Ligningen løses for s vha. WordMat.*

So actually this circuit has 2 repeated roots at

Further approximations can be held, if we assume that C1 ≈ C2, R1 ≈ R2 then

Describing the system from that I use  
Where A0 will be my DC gain. And that I calculated in task a.   
   
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